Development of the ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC

Mathis Kolb⋆ on behalf of the ATLAS Liquid Argon Calorimeter Group

IRFU, CEA, Université Paris-Saclay, France

⋆ mathis.kolb@cern.ch

Proceedings for the XXVIII International Workshop on Deep-Inelastic Scattering and Related Subjects, Stony Brook University, New York, USA, 12-16 April 2021
doi:10.21468/SciPostPhysProc.8

Abstract

The full ATLAS Liquid Argon Calorimeter electronic readout chain will be upgraded for the high-luminosity LHC. The upgrade is designed to withstand the expected radiation level and to be compatible with the Phase-I Digital Trigger System which is being installed right now. Analogue electronics shape and amplify the calorimeter signals before they are digitized with 16 bit dynamic range on two gain scales. The on-detector system samples the calorimeter cell signals at 40 MHz and sends them to the off-detector electronics which apply digital processing based on FPGAs. Design studies and tests of prototypes of the upgraded components are presented.

Received 29-07-2021
Accepted 22-03-2022
Published 14-07-2022
doi:10.21468/SciPostPhysProc.8.158

1 Introduction

The Large Hadron Collider (LHC) [1] will undergo a luminosity upgrade to the high-luminosity LHC (HL-LHC) in the next years. The HL-LHC is expected to achieve an integrated luminosity of 4000 fb^{-1} under a pile-up rate of $2-5$ times higher than presently, i.e. up to 200 proton-proton collisions per bunch crossing at the ATLAS experiment [2]. As a consequence the detector readout electronics will suffer faster ageing than today due to the high level of radiation. The ATLAS trigger and data acquisition (TDAQ) system will evolve to a new architecture with 10 μs latency and a rate of 1 MHz at the hardware trigger level [3]. An upgrade of the Liquid Argon calorimeter (LAr) readout electronics during the ATLAS Phase-II upgrade is required to achieve the expected performance [4]. The schematic block diagram of the LAr calorimeter readout architecture for the Phase-II upgrade is shown in Figure 1. The on-detector electronics are placed on the cryostat signal feedthroughs inside the ATLAS detector. The off-detector electronics are installed in Advanced Telecommunications Computing Architecture (ATCA) shelves located underground close to the detector. An overview of the development of the upgraded LAr electronic components at on-detector and off-detector level is presented in the following.

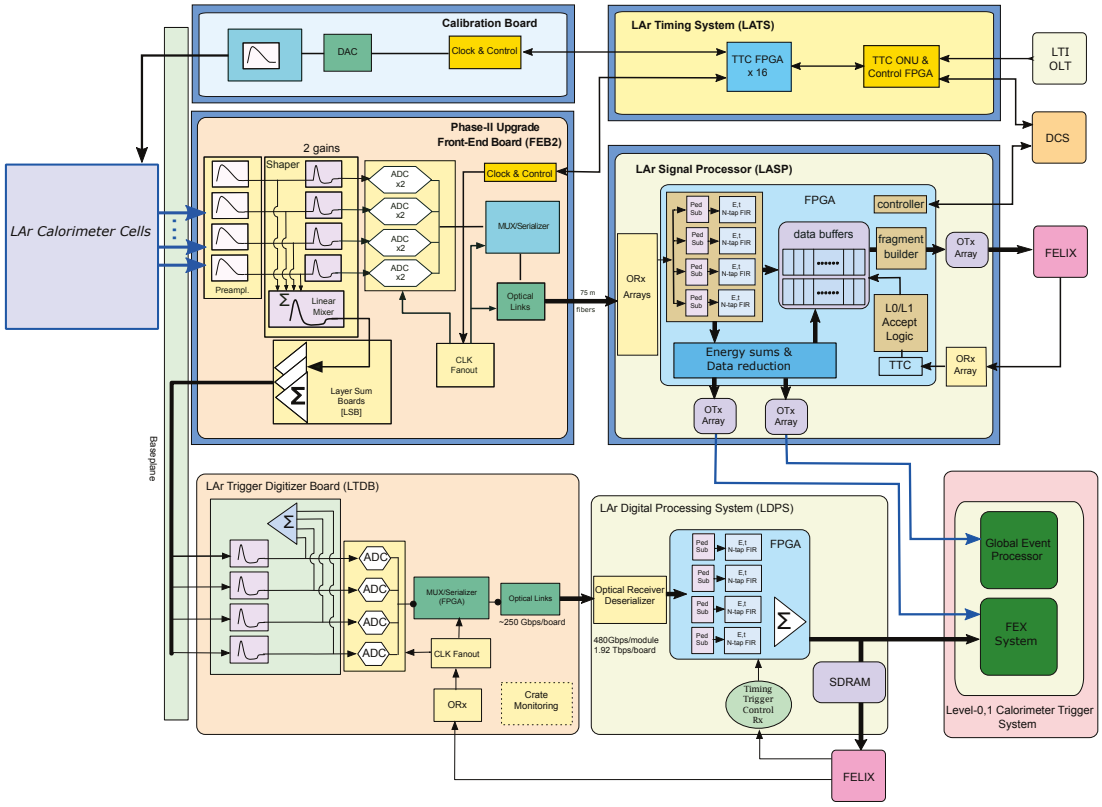

Figure 1: Schematic overview of the LAr calorimeter readout architecture for the Phase-II upgrade. The LAr Trigger Digitizer Board (LTDB) and LAr Digital Processing System (LDPS) are part of the Phase-I upgrade and will remain for Phase-II.

2 On-detector electronics

The Phase-II upgrade of the on-detector electronics contains the new Front-end Board (FEB2) and the calibration board. Each FEB2 contains 128 readout channels. The total readout system consists of 1524 FEB2 boards and 122 calibration boards. The physics requirements demand a large dynamic range from energies produced by minimum ionizing particles up to energies of several TeV which can for example occur in searches for new physics. The reduced number of two gain scales, compared to three scales in the current readout chain, with a threshold further away from electron and photon energies from Z boson and Higgs boson decays will help in precision measurements.

2.1 Calibration board

The calibration system provides a pulse of known amplitude and shape which is injected directly on calorimeter cells. This allows one to probe the electronic response of each calorimeter channel. Each board contains 128 channels. The calibration system has to fulfill an integrated non linearity (INL) below 0.1%, a fast pulse rise time below 1 ns, 16-bit dynamic range and it must be radiation hard up to 180 kRad. The dynamic range of the pulse up to 7.5 V requires a HV-CMOS technology. The pulser and the digital to analog (DAC) component are implemented on two separate ASICs. The CLAROC (Calibration of Liquid ARgon Output Chip) chip version 3 is based on XFAB HV-CMOS 180 nm technology and contains the high-frequency switch and current mirrors. The 16-bit DAC is implemented on the LADOC (Link And DAC of CLAROC)

chip using TSMC 130 nm CMOS technology. Each ASIC can handle four channels. Tests are performed on this prototype to check if it fits the specifications. The 32-channel board CABANON (CAlibration Board with 32-chANnels for demonstratiON) has also been developed and is being tested.

2.2 Front-end board

The FEB2 boards perform analogue processing and digitization of the calorimeter signals. In a first stage the signal is amplified, shaped and split in two linear gain scales. In a second stage the ADC digitizes the low and the high gain scale at 40 MHz. The digitized data are formatted, multiplexed and sent off detector via optical links. The FEB2 is made of 32 Preamplifier/shaper (Pa/Sh) ASICs, 32 ADC ASICs, 24 serializer chips (lpGBT) and 8 optical modules (VTRX+). Furthermore, Layer Sum Boards (LSBs) connect the main readout with the Phase-I Digital Trigger System. The LSBs produce the analogue trigger sums which are sent to the Phase-I LAr Trigger Digitizer Boards (LTDB). First LSB test boards were received and the basic functionality is working.

2.2.1 Preamplifier-Shaper

The analogue processing of the signals consists of amplification, applying a CR$-$(RC)^2 shaping function on the detector pulse and splitting the signal on two overlapping gain scales with a gain ratio of around 23. This functionality is achieved by both prototype ASICs (ALFE (ATLAS Liquid Argon Front-End) and LAUROC (Liquid Argon Upgrade Readout Chip)) developed in 130 nm CMOS technology. They can handle four channels per ASIC and have a dynamic range larger than 16-bit. A highly configurable design relying on the I^{2}C interface is implemented. The main requirements in terms of e.g. INL below $\pm$0.2% on the high gain output, equivalent noise current (ENI) below 350 nA (120 nA) for a 25 Ω (50 Ω) termination and power-supply rejection ratio (PSRR) above +10 dB up to 1 MHz are met and the final prototype (ALFE) is submitted for fabrication.

2.2.2 ADC

The ADC ASIC digitizes the data on the two gain scales with four calorimeter channels per ASIC. The ADC digitizes signals on a 14-bit dynamic range with two gains to cover the 16-bit dynamic range. It has to achieve a noise level well below the intrinsic LAr resolution and per-mille level linearity at the electroweak scale to meet the physics requirements. An Effective Number of Bits (ENOB) of at least 11 bits guarantees that the LAr energy resolution can be maintained. The designed ADC ASIC (COLUTA) implements a 40 MHz pipeline ADC with Multiplying DAC (MDAC) in combination with a 12-bit pipeline Successive Approximation Register (SAR) ADC developed in 65 nm CMOS technology. The pre-prototype COLUTA version three implements four MDAC plus SAR channels and four additional test channels on the ASIC. The chip is configurable with the I^{2}C interface. It meets the requirements on the power consumption per channel and the radiation hardness. An ENOB above 11 is measured for the relevant frequency range. The future COLUTA version 4 design will provide the full 8 MDAC plus SAR channels functionality.

2.2.3 Integration

Several stages of FEB2 prototype boards were developed with increasing complexity. The first version, called analogue test board, contains two channels and pre-prototype versions of all components. Tests based on that board confirm that the readout chain is correctly working.

The second version, dubbed slice test board, features 32 channels and updated ASICs. Control functionality and the readout are tested on the slice test board and the multi-channel performance is demonstrated.

3 Off-detector electronics

The off-detector electronics will comprise around 20 LAr Timing System (LATS) boards and 380 LAr Signal Processor (LASP) boards. The LASP handles the digital signal processing and sends output data to the Phase-I LDPS and to the TDAQ system. The LATS provides the Timing, Trigger and Control interface (TTC) to the on-detector electronics.

3.1 LAr Timing System

The LATS distributes the TTC signals to the FEB2 and calibration boards and handles the configuration and monitoring. A dedicated board, called Liquid Argon Timing trigger cOntroldistribUtion and fRoNt End moniToring/ConfiguraTion (LATOURNETT), is developed for that purpose. The functionality will be achieved by an ATCA board with a control FPGA and 16 FPGAs for the TTC. At the current stage the power tree of the board is designed and first PCBs are received for assembly. The firmware is developed in parallel with a Cyclone 10 development kit and a FPGA mezzanine card that allows one to emulate external optics, the FPGA links and the clock distribution.

3.2 LAr Signal Processor

The LASP receives the digitized data from the FEB2 and performs digital filtering on it. Each LASP board processes around 512 readout channels. The ATCA main blade hosts two FPGAs which apply pile-up correction, calculate the calibrated energies and the signal time. The data is buffered and eventually sent to the TDAQ system. The FPGA firmware development relies on continuous integration and automatic simulation. Dedicated test boards are developed to validate the firmware implementation. The pre-prototype of the LASP board is in the fabrication stage. A rear transmission module (RTM) adds a controller FPGA and optical transceivers. The RTM pre-prototype is available and related firmware development has started.

4 Conclusion

The luminosity upgrade of the LHC requires the development of a new readout chain for the LAr calorimeter at the ATLAS experiment. Custom radiation tolerant ASICs are designed and tested. The prototypes of the on-detector signal processing meet the specification requirements at the HL-LHC. The interplay between the on-detector components was successfully validated with FEB2 pre-prototype boards implementing a reduced number of readout channels per board. The off-detector functionality is realized by ATCA boards with different FPGAs. The digital filtering is performed on the LASP board for which the pre-prototype fabrication started. Firmware is implemented in parallel using dedicated test boards.

References

[1] L. Evans and P. Bryant, *LHC Machine*, J. Inst. **3**, S08001 (2008), doi:10.1088/1748-0221/3/08/s08001.

[2] ATLAS Collaboration, *The ATLAS Experiment at the CERN Large Hadron Collider*, J. Inst. **3**, S08003 (2008), doi:10.1088/1748-0221/3/08/S08003.

[3] ATLAS Collaboration, *Technical Design Report for the Phase-II Upgrade of the ATLAS TDAQ System*, ATLAS-TDR-029.

[4] ATLAS Collaboration, *ATLAS Liquid Argon Calorimeter Phase-II Upgrade: Technical Design Report*, ATLAS-TDR-027.